

Date : 2003, 8, 1

Technical Data Sheet

96 Column × 64 Row 65K Color OLED

■ SUPPLIER APPROVAL

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August, 1, 2003

PRELIMINARY Ver. 1.0

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1. GENERAL DESCRIPTION

This display module is 288 segments ($96 \times \text{RGB}$) and 64 commons pixel OLED graphic display control through an 8-bit parallel interface and requiring a dual voltage power supply.

The module are sent from general MCU through the hardware selectable 6800/8080 series compatible parallel interface or serial peripheral interface. It has a 256 steps contrast control and 65 color control.

2. FEATURES

- Support max. $96 \times \text{RGB} \times 64$ matrix panel
- Power supply : $V_{DD}=2.4\text{V}-3.5\text{V}$
 $V_{CC}=8.0\text{V}-18.0\text{V}$
- OLED driving output voltage, 11V maximum
- DC-DC voltage converter
- Segment maximum source current : 200uA
- Common maximum sink current : 50mA
- Embedded $96 \times 64 \times 16$ bit SRAM display buffer
- 16 step master current control, and 256 step current control for the three color components
- Programmable Frame Rate
- Graphic Acceleration Command Set (GAC)
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral Interface.
- Wide range of operating temperature : -30 to 85°C

3. MECHANICAL SPECIFICATION

ITEM	STANDARD SIZE	UNIT
Dimensional outline	27.8(W)x24.3(H)x1.65(T)	mm
Number of dots	96(W)xRGBx64(H)	dots
Viewing area	24.143(W)x18.274(H)	mm
Active area	20.997(W)x16.04(H)	mm
Pixel size	0.046(W)x0.227(H)	mm
Pixel pitch	0.073 W) x0.251(H)	mm
Weight	3	g
Glass thickness	0.7	mm

4. ABSOLUTE MAXIMUM RATINGS

ITEM		SYMBOL	MIN	MAX	UNIT
Supply voltage	Logic	Vdd	- 0.3	4.0	V
	Driving	Vcc	-0.3	11.0	V
Operating temperature range		Topt	-20	70	°C
Storage temperature range		Tstg	-30	85	°C
Humidity				95	%RH

5. ELECTRICAL CHARACTERISTICS

ITEM		SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply Voltage	Logic	Vdd	(1)	2.4	2.7	3.5	V
		Vdd	(2)	2.4	2.7	3.5	V
	Driving	Vcc	(2)	10.5 ~ 11			V
Input Voltage	High	VIH	(1)(2)	0.75xVdd	-	Vdd	V
	Low	VIL	(1)(2)	0	-	0.15xVdd	V
Input Current	Logic	Idd	(1)	-	0.9	2.0	mA
		Idd	(2)	-	0.9	2.0	mA
	Driving	Icc	(1)	-	7	10	mA
		Icc	(2)	-	20	24	mA

Condition :

- (1) Under the condition of Luminance=45cd/m², Vdd=3.3V, Ta=25°C the Vcc=8 V, the command set value as following:

Contrast for Color A (81h)=(1C),

Contrast for Color B (82h)=(07),

Contrast for Color C (83h)=(FF),

Master Current Control (87h)=0F

- (2) Under the condition of, Vcc=11V, Vdd=3.3V, Ta=25°C the luminance=100cd/m², the command set value as following:

Contrast for Color A (81h)=(20),

Contrast for Color B (82h)=(08),

Contrast for Color C (83h)=(FF),

Master Current Control (87h)=0F

6. ELECTRO-OPTICAL CHARACTERISTICS

ITEM		MIN	TYP	MAX	UNIT
Initial Luminance	White(1)	35	45	55	cd/m ²
Initial Luminance	White(2)	90	100	110	cd/m ²
Contrast Ratio	White/black(3)	200			
C.I.E	White	X	0.26	0.29	0.32
		Y	0.35	0.38	0.41
	Red	X	0.55	0.58	0.61
		Y	0.36	0.39	0.42
	Green	X	0.25	0.28	0.31
		Y	0.52	0.55	0.58
	Blue	X	0.10	0.13	0.16
		Y	0.20	0.25	0.30
Life Time	White(1)			5000	HR
	White(2)			3500	HR

Condition :

- (1) Under the condition of Luminance=45cd/m², Vdd=3.3V, Ta=25°C, the Vcc=8 V, the command set value as following:

Contrast for Color A (81h)=(1C),
 Contrast for Color B (82h)=(07),
 Contrast for Color C (83h)=(FF),
 Master Current Control (87h)=0F

- (2) Under the condition of, Vcc=11V, Vdd=3.3V, Ta=25°C, the luminance=100cd/m², the command set value as following:

Contrast for Color A (81h)=(20),
 Contrast for Color B (82h)=(08),
 Contrast for Color C (83h)=(FF),
 Master Current Control (87h)=0F

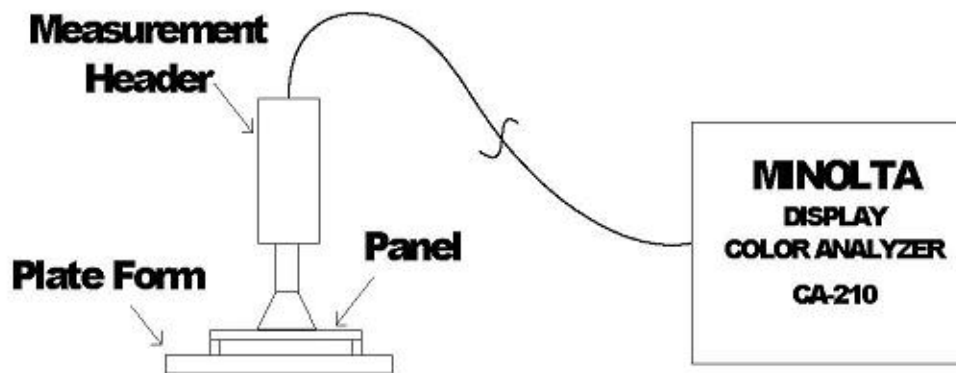
(3) Contrast Ratio (under the condition of 100 cd/m²)

$$\text{Contrast Ratio} = \frac{\text{Brightness at selected segment (display at white area)}}{\text{Brightness at unselected segment (display at black area)}}$$

(4) Life-time : The period of time that the initial luminance decay 50% under the condition of continuous driving in full white color.

Notice :

The optical testing system of Luminance, C.I.E and contrast ratio

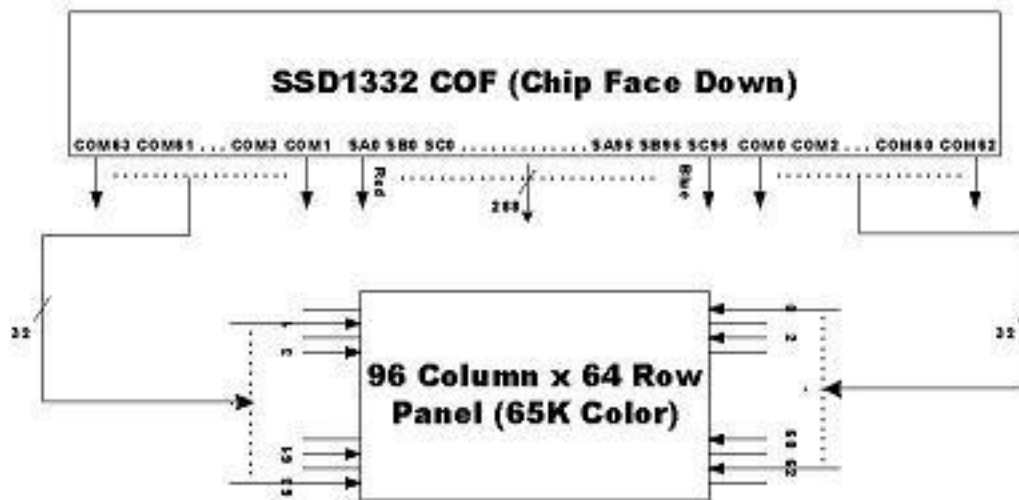


7. INTERFACE PIN DESCRIPTION

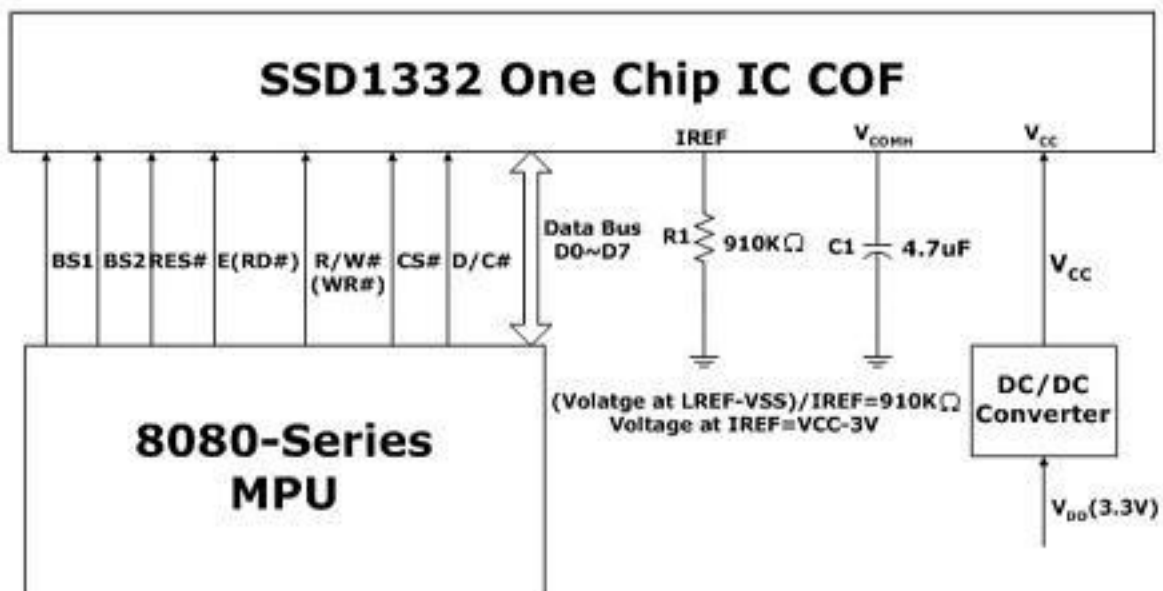
No.	TYPE	NAME	DESCRIPTION
1		N.C.	Non connect
2	P	V _{cc}	Driving OLED
3	P	V _{COMH}	Driving COM signals Voltage
4		N.C.	Non connect
5	I/O	D7	Data Bus
6	I/O	D6	Data Bus
7	I/O	D5	Data Bus
8	I/O	D4	Data Bus
9	I/O	D3	Data Bus
10	I/O	D2	Data Bus
11	I/O	D1	Data Bus
12	I/O	D0	Data Bus
13	I	#RD	Read Enable clock Input pin
14	I	#WR	Write Enable clock Input pin
15	I	#D/C	Data/Command control pin
16	I	#RES	Rest signal input
17	I	#CS	Chip select input
18	I	I _{REF}	Reference for OLED driving current
19	I	BS2	MCU interface select input
20	I	BS1	MCU interface select input
21	P	V _{DD}	OLED driving voltage
22	P	V _{P-C}	Driving segment signals for SCO-SC95
23	P	V _{P-B}	Driving segment signals for SCO-SB95
24	P	V _{P-A}	Driving segment signals for SCO-SA95
25		V _{BREF}	Testing
26		RESE	Testing
27		FB	Testing
28	P	V _{DDBUF}	Power supply pin for DC-DC converter
29		GDR	Testing
30		V _{SS}	Ground
31		N.C.	Non connect

8. BLOCK DIAGRAM

8-1 Circuit Block Diagram

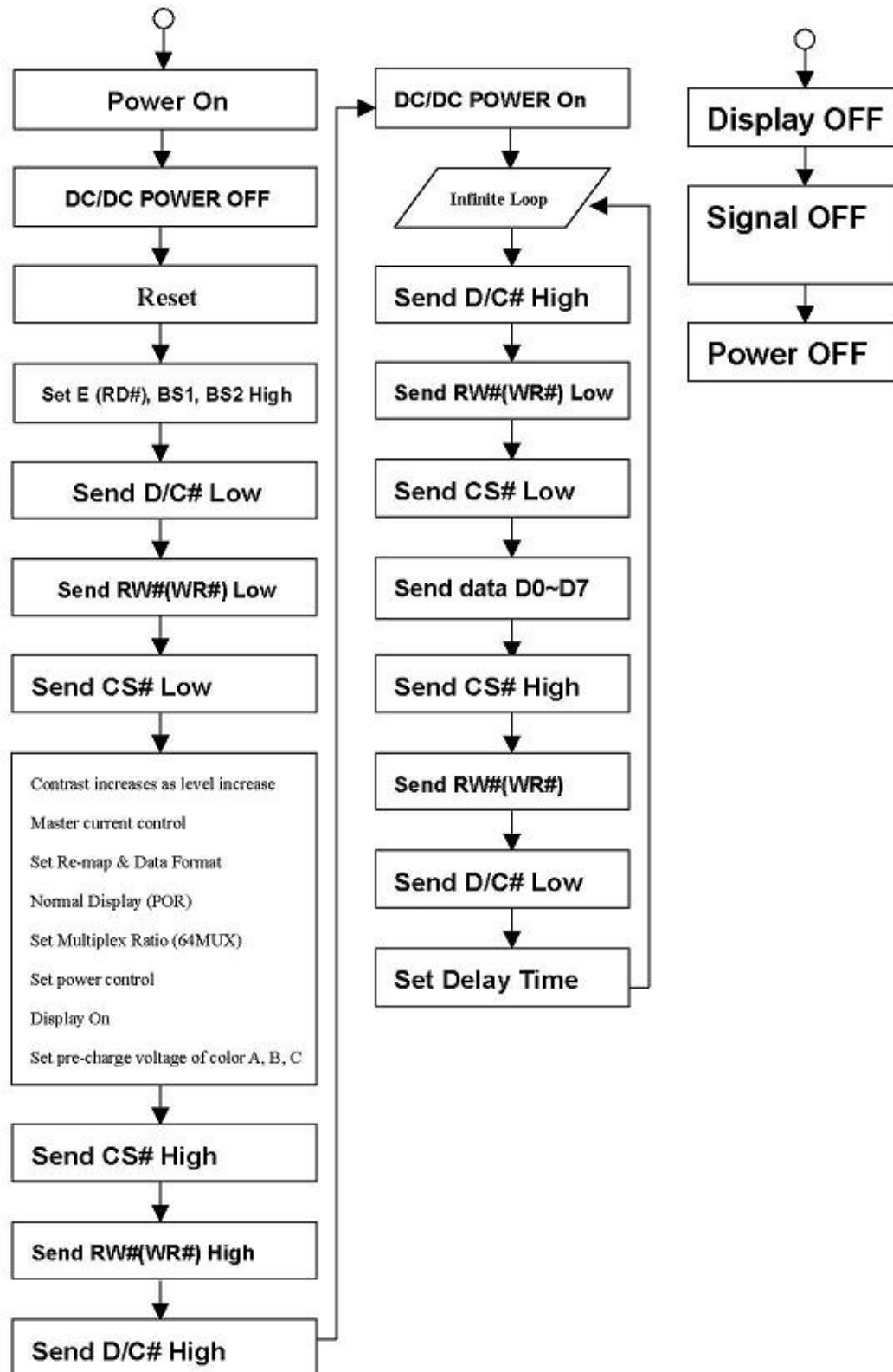


8-2 MPU Interface



9. TIMING CHARACTERISTIC

9-1 Power ON/OFF Sequence



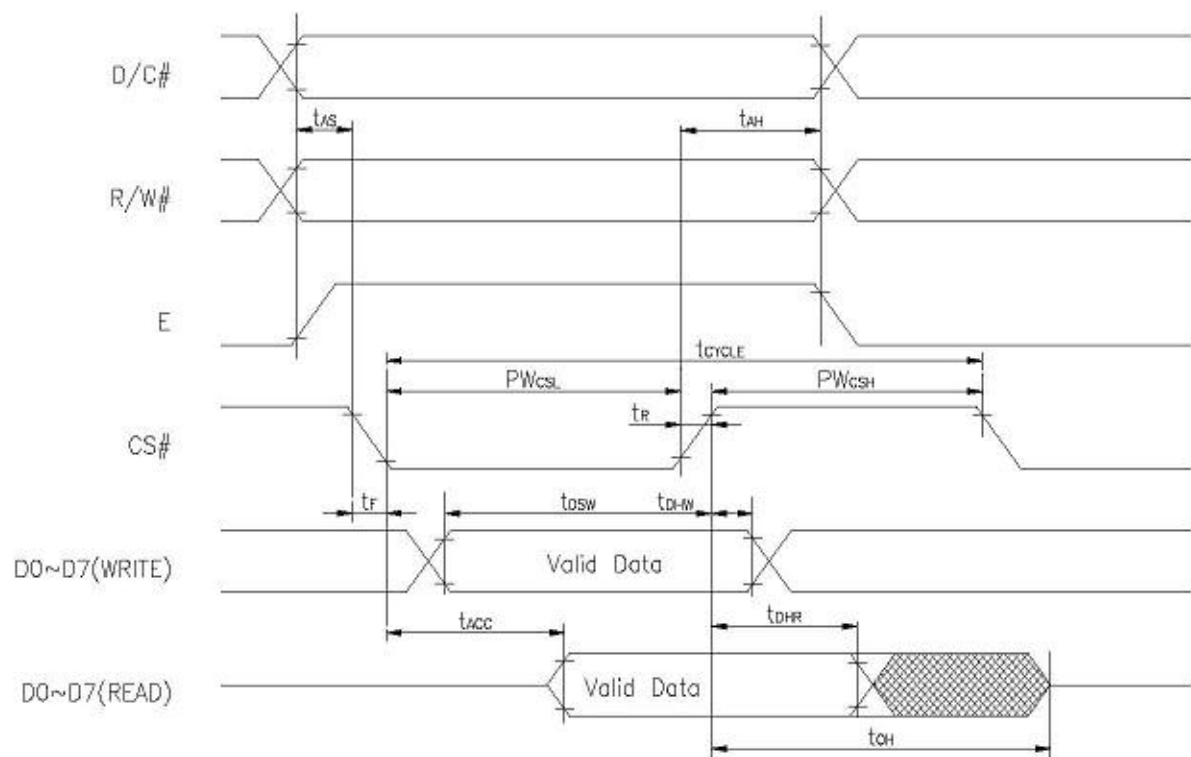
9-2 Command Sequence

Instruction		Code	Description
Set Command Sequence			
1	Set Column Address	00010101	Set Column Address
2	Set the column start address	00000000	Second command A [7:0] sets the column start address from 0-95, POR=00d.
3	Set the column end address	01011111	Third command B [7:0] sets the column end address from 0-95 POR=95d.
4	Set Row Address	01110101	Set Row Address
5	Set the Row start address	00000000	Second command A [6:0] sets the row start address from 0-63, POR=00d.
6	Set the Row end address	00111111	Third command B [6:0] sets the row end address from 0-63, POR=63d.
7	Set Contrast for Color A	10000001	Double byte command to select 1 out of 256 contrast steps. Contrast increases as level increase. POR = 80H
		00010101	
8	Set Contrast for Color B	10000010	Same as above
		00000011	
9	Set Contrast for Color C	10000011	Same as above
		00010101	
10	Master Current Control	10000111	Set A [3:0] from 0000, 0001... to 1111 to adjust the master current attenuation factor from 1/16, 2/16... to 16/16. POR = 1111b, for no attenuation.
		00001111	
11	Set Re-map & Data Format	10100000	Set Re-map & Data Format
		01000000	
12	Set Display Mode	10100100	Normal Display (POR)
13	Set Multiplex Ratio	10101000	Set Multiplex Ratio (64MUX)
		00111111	
14	Set Power Control	10101001	Display on, Enable Oscillator
		00001010	
15	Set Display On/Off	10101111	Display On

9-3 Read/ Write Characteristic (6800-series, MPU)

($V_{DD} - V_{SS} = 2.4$ to $3.5V$, $T_A = -30$ to $85^\circ C$)

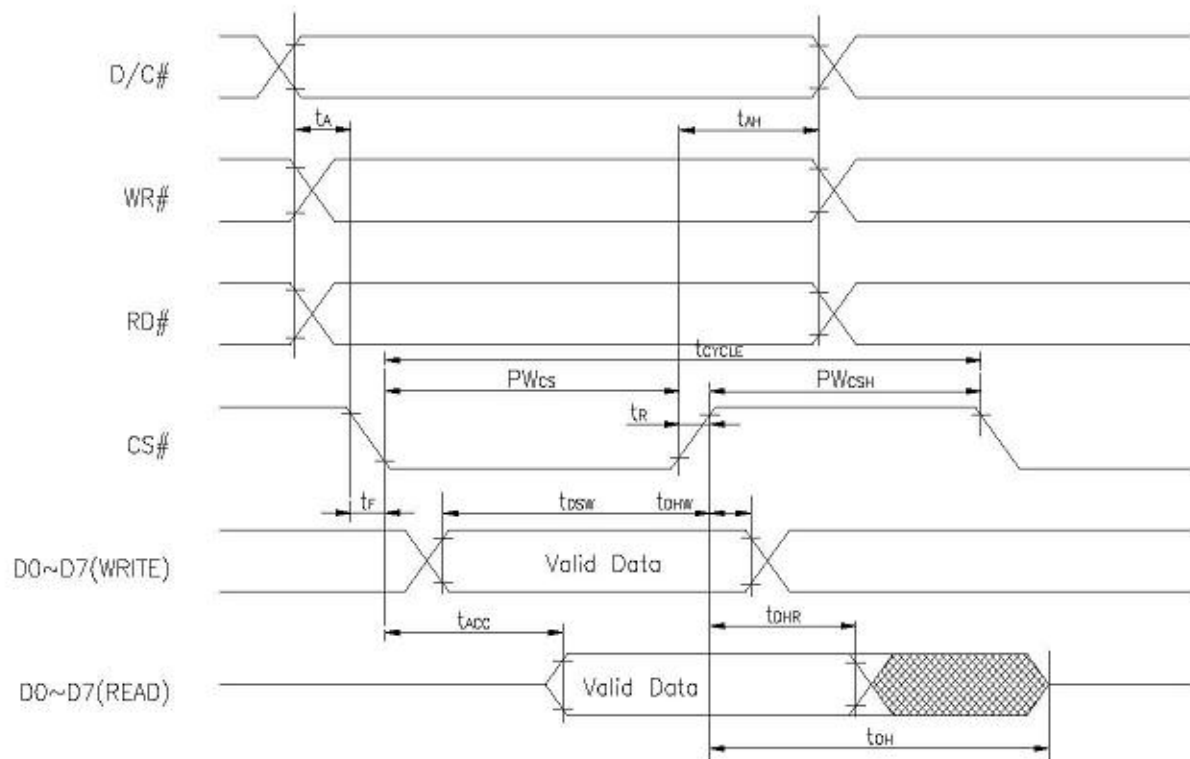
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read)	120	-	-	ns
	Chip Select Low Pulse Width (write)	60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read)	60	-	-	ns
	Chip Select High Pulse Width (write)	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



9-4 Read/ Write Characteristic (8080-series, MPU)

($V_{DD} - V_{SS} = 2.4$ to $3.5V$, $T_A = -30$ to $85^\circ C$)

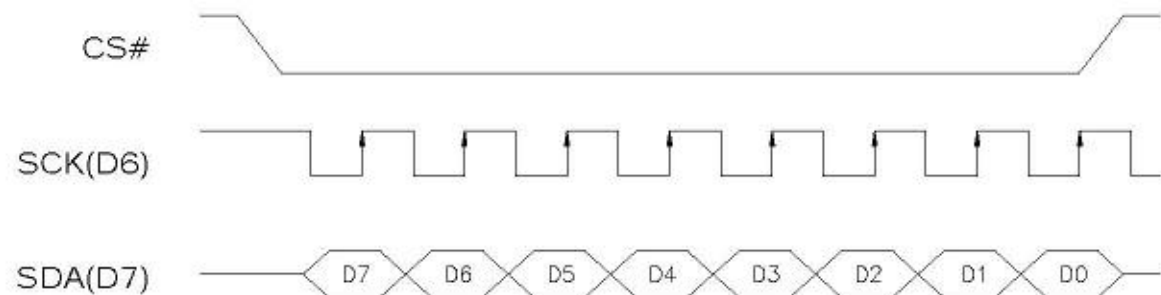
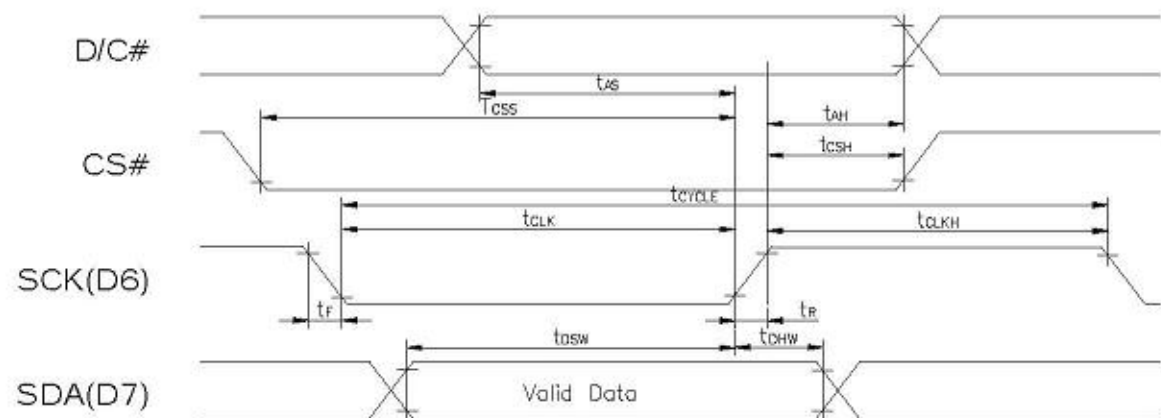
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read)	120	-	-	ns
	Chip Select Low Pulse Width (write)	60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read)	60	-	-	ns
	Chip Select High Pulse Width (write)	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



9-5 Serial Interface Characteristic

($V_{DD} - V_{SS} = 2.4$ to $3.5V$, $T_A = -30$ to $85^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



9-6 COMMAND TABLE

(D/C# =0, R/W#(WR#)=0, E(RD#)=1)

Hex	Command	Description
15 A[6:0] B[6:0]	Set column Address	Second command A [7:0] sets the column start address from 0-95, POR=00d. Third command B[7:0] set the column end address form 0-95 POR=95d.
75 A[5:0] B[5:0]	Set Row Address	Second command A [6:0] sets the row start address from 0-63, POR=00d. Third command B[6:0] set the row end address form 0-63 POR=63d.
81 A[7:0]	Set Contrast for Color A (Segment Pins: SA0-SA95)	Double byte command to select 1 out of 256 contrast steps. Contrast increases as level increase. POR=80H.
82 A[7:0]	Set Contrast for Color B (Segment Pins: SB0-SB95)	Same as above
83 A[7:0]	Set Contrast for Color C (Segment Pins: SC0-SC95)	Same as above
87 A[3:0]	Master Current Control	Set A [3:0] from 0000,0001... to 1111 to adjust the master current attenuation factor 1/16,2/16...to 16/16. POR=1111b, for no attenuation
A0 A[7:0]	Set Re-map & Data Format	A[0]=0, Horizontal address increment (POR) A[0]=1, Vertical address increment A[1]=0, Column address 0 is mapped to SEG0 (POR) A[1]=1, Column address 131 is mapped to SEG0 A[2]=0, Reserve A[3]=0, Reserve A[4]=0, Scan from COM 0 to COM [N-1] A[4]=1, Scan from COM [N-1] to COM 0. Where N is the Multiplex ratio. A[5]=0, Disable COM split Odd Even (POR) A[5]=1, Enable COM split Odd Even A[7:6]=00; 256 color format = 01; 65k color format Data formats are defined as CCCBBA for 256 color CCCCBBB for 65K color BBBAAAA

Hex	Command	Description
A1 A[5:0]	Set Display Start Line	Set display RAM display start line register form 0-63 Display start line register is reset to 00H after POR.
A2 A[5:0]	Set Display Offset	Set vertical scroll by COM from 0-63. The value is reset to 00H after POR.
A4~A7	Set Display Mode	A4H-Normal Display (POR) A5H-Entire Display On, all pixels turn on at GS level 63 A6H-Entire Display Off, all pixels turn off A7H=Inverse Display
A8 A[5:0]	Set Multiplex Ratio	The next command determines multiplex ratio N form 16MUX-64MUX, POR=63d (64MUX)
A9 A[5:0]	Set Power Control	A[0]=0, Display OFF (POR) A[0]=1, Display ON A[1]=0, Disable oscillator A[1]=1, Enable oscillator (POR) A[2]=0, Reserve A[3]=0, Reserve A[4]=0, Reserve A[5]=0, Reserve
AE~AF	Set Display On/Off	AEH=Display off (POR) AFH=Display on
B8 A[7:0] –PW1 B[7:0] –PW3 C[7:0] –PW5 D[7:0] –PW7 : : AE[7:0] –PW61 AF[7:0] –PW63	Set Gray Scale Table	The next 32 bytes of command set the current drive pulse width of gray scale level GS1, GS3, GS5...GS63 as below: A[7:0]=PW1, POR=1 B[7:0]=PW3, POR=5 C[7:0]=PW5, POR=9 : AE[7:0]=PW61, POR=121 AF[7:0]=PW63, POR=125 Note: GS0 has no current drive. For GS2 GS4...GS62: $PW_n = (PW_{n-1} + PW_{n+1})/2$ Max pulse width is 125
E3	NOP	Command for No Operation

9-7 COMMAND DESCRIPTIONS

Set Column Address

This command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address.

Set Row Address

This command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address.

Set Contrast for Color A, B, C

This command is to set Contrast Setting of each color A, B and C. The chip has three contrast control circuits for color A, B and C. Each contrast circuit has 256 contrast steps form 00H to FFH. The segment output current increases linearly with the increase of contrast step.

Master Current Control

This command is to adjust the overall display brightness. The chip has 16 steps segment current reduction. The range is form 1/16[0000] to 16/16 [1111]. POR is no current reduction [1111].

Set Re-map

This command changes the mapping between the display data column address and segment driver, row address and common driver. It allows flexibility in layout during OLED module assembly.

When A[5] is set as 0, COM outputs are in sequential format. When it is set as 1, COM outputs are in odd and even mode.

Set Data Format

This command allows user to set different data formats for 256 color (8-bit) and 65k color(16-bit).

Set Display Start Line

This command is to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 63.

Set Display Offset

This is a double byte command. The next command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0-63. For example, to move the COM16 towards the COM0 direction for 16 lines, the 6-bit data in the second command should be given by 0010000.

Set Display Mode

This command is used to set Normal Display, Entire Display On, Entire Display Off and Inverse Display. Set Entire Display On forces the entire display to be at "GS63" regardless of the contents of the display data RAM. Set Entire Display Off forces the entire display to be at gray level "GS0" regardless of the contents of the display data RAM. Normal Display will turn the data to ON at the corresponding gray level.

Set Multiplex Ratio

This command switches default 1:64 multiplex mode to any multiplex mode from 16 to 64.

Set Display On/Off

This command turns the display on or off. When the display is off, the segment and common output are in high impedance state.

Set Gray Scale Table

This command is used to set the gray scale table for the display. Except GS0, which has no pre-charge and current drive, each GS level is programmed by the pulse width of current drive.

NOP

No Operation Command

10. QUALITY SPECIFICATION

10-1 Acceptable Quality Level

Inspection item	Sampling procedures	A.Q.L
Major	MIL-STD-105E Level II Normal Inspection Single sample inspection	0.65
Minor	MIL-STD-105E Inspection Level II Normal Inspection Single sample inspection	1.0

➤Major defect:

A major defect is a defect that could result in failure or materially reduce that the usability of the unit of product for its intended purpose.

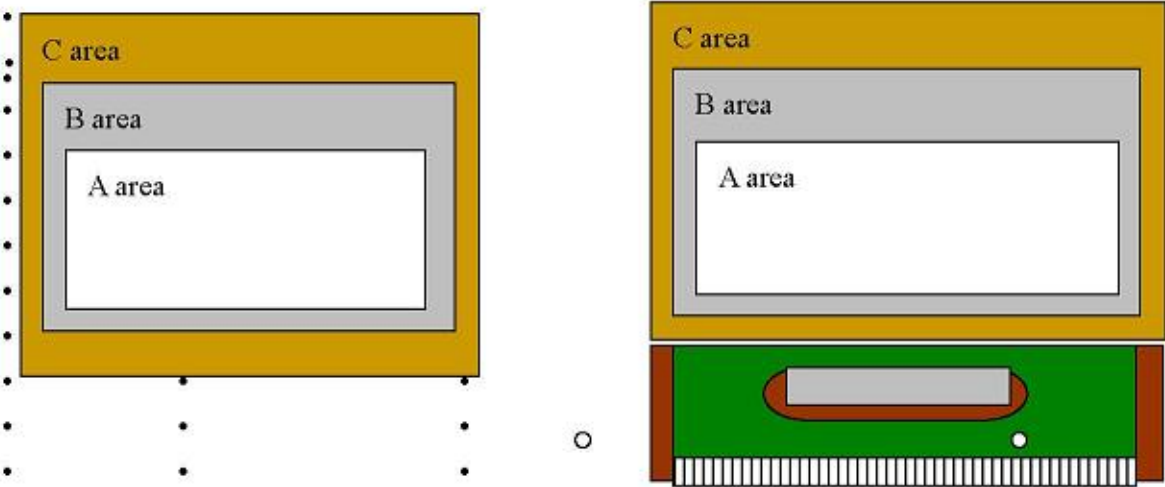
➤Minor defect:

A minor defect is one that dose not materially reduce the usability of the product for its intended purpose or is a departure from established standards giving no significant bearing on the effective use or operation of the unit.

10-2 Inspection Conditions

- 10.2.1 The environmental conditions for inspection shall be as follows
- Room Temperature: $25 \pm 3^{\circ}\text{C}$
 - Humidity Temperature: $65 \pm 20\% \text{ RH}$
 - Clear room level 1000
- 10.2.2 The external visual inspection
- The inspection shall be performed by using 40 Watts fluorescent lamp for illumination and the distance between panel and eyes of the inspector shall be 30cm or more.

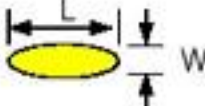
10-3 Definition of the Area



- A:Active Area •
- B:Viewing Area •
- C:Out of Viewing Area •
- •

- • •
- • •
- • •
- • •

10-4 Inspection Standards

Class of defects	Inspection defects Item	Criteria		AQL
Major	Display on inspection	1) No Display		0.65
		2) Abnormal Operation		
		3) Short Circuit		
		4) Missing vertical, Horizontal segment		
	Missing	Component missing		
Minor	Spots / Dent Φ..... 	Defect size (mm)	Acceptable Number	1.0
		Φ.....	Ignore	
		 Φ.....	3	
		 Φ.....	2	
		 Φ.....	1	
		Φ.....	0	
	Scratch	Width * Length (mm)	Acceptable Number	
		<= W0.018 * L 1.5	Ignore	
		0.018<W<=0.02 (L<=1.5)	3	
		0.02< W<=0.03 (L<=3.0)	2	
		0.03< W<=0.05 (L<=3.0)	1	
		W > 0.05 or (L > 3.0)	0	

10-5 Reliability Test Condition

Item	Condition	Inspection Standard	Inspection Standard
Storage	High temperature	85°C, 96 hours	1. After testing, the exterior or character defect is not allowed 2. Total current consumption should be below double of initial value 3. After testing, the contrast ratio should be more than 100 4. After testing, the luminance can't decay over 50%
	Low temperature	-30°C, 96 hours	
	High temp/humidity	••°C, 95%RH, 96 hours	
	Thermal shock	••°C/-30°C (30m/15m), 10cycles	
Operating	High temperature	70°C, 96 hours	1. After testing, it must be in range of the initial CIE volume 2. Exterior electrical defect is not allowed 3. Total current consumption should be below double of initial value.
	Low temperature	-20°C, 96 hours	
	High temp/humidity	••°C, 90%RH, 96 hours	
	Thermal shock	••°C/-30°C (30m/15m), 10cycles	
	Vibration		
	ESD	Ω±.....	

Note:

❶ ESD

Although the function obstacle occurred because of ESD damage, if after resetting and the function return to normal, it is still considered as normal.

❷ Cross Talk

The cross talk will appear under the black box pattern with white-color background and under the white box with black-color background. But cross talk will not appear under the time pattern with black-color background. If the operation voltage were over 11 voltage, cross talk may be appear.

❸ Flicker

Flicker will appear under the condition of R, G, B and white pattern fully lighten and the white-color background. When the frame increases, the flicker will reduce. If turn the frame from 60Hz to 90Hz, the condition of flicker will be improved but the brightness will decrease.

❹ Luminance Difference

The different luminance between right and left side could be recognized under the condition of R, G, B and white pattern, but it will not appear under the black-color background.

❺ Remaining Picture

Because the dots are lighten in different time and may reduce the luminance or cause the different luminance from surrounding unused dots so that the remaining picture will occur.

Because of the above description, every dot on panel needs to be used.

...

11 MATTERS NEEDING ATTENTION

11-1 Package

- ❶ OLED module should be kept under the condition of packing when it is shipped. While opening the package, the following items should be noticed.
- ❷ OLED module consists of glass; it should be prevented from heavily pressing and dropping from high place.
- ❸ The panels should be prevented from exposing to direct sunlight, high temperature and high humidity for a long time
- ❹ Refrain from discharge of high electro-static voltage.

11-2 Driving

- ❶ The order of turning on the current must from Vdd to Vcc
The order of turning off the current must from Vcc to Vdd
- ❷ If the input voltage is over provided operating (driving) voltage range, it will reduce the life hours of OLED panel
- ❸ The panel should be operated within the range of temperature and humidity mentioned in the data sheet, otherwise, it may cause chemical reaction
- ❹ Please do not pull, twist or bend the connector and cable used for OLED module
- ❺ Panel and connector should be pasted or stuck together accurately
- ❻ Please drive the panel with the normal on or off, if it is not driven according to the normal procedure, OLED panel may be damaged or can not be restored.
- ❼ When the DC signals increase, it also may cause the damage of OLED panel.

11-3 Panel Cleaning

- ❶ If it is necessary to deal with the surface of OLED panel, please use the Ethyl alcohol and Isopropyl alcohol.
- ❷ ITO pad cannot be cleaned by hard stuff and Soldering flux, Chlorine, Sulfur, Spittle or Fingerprint.

11-4 Before Using

The following situation should be handled by OSD:

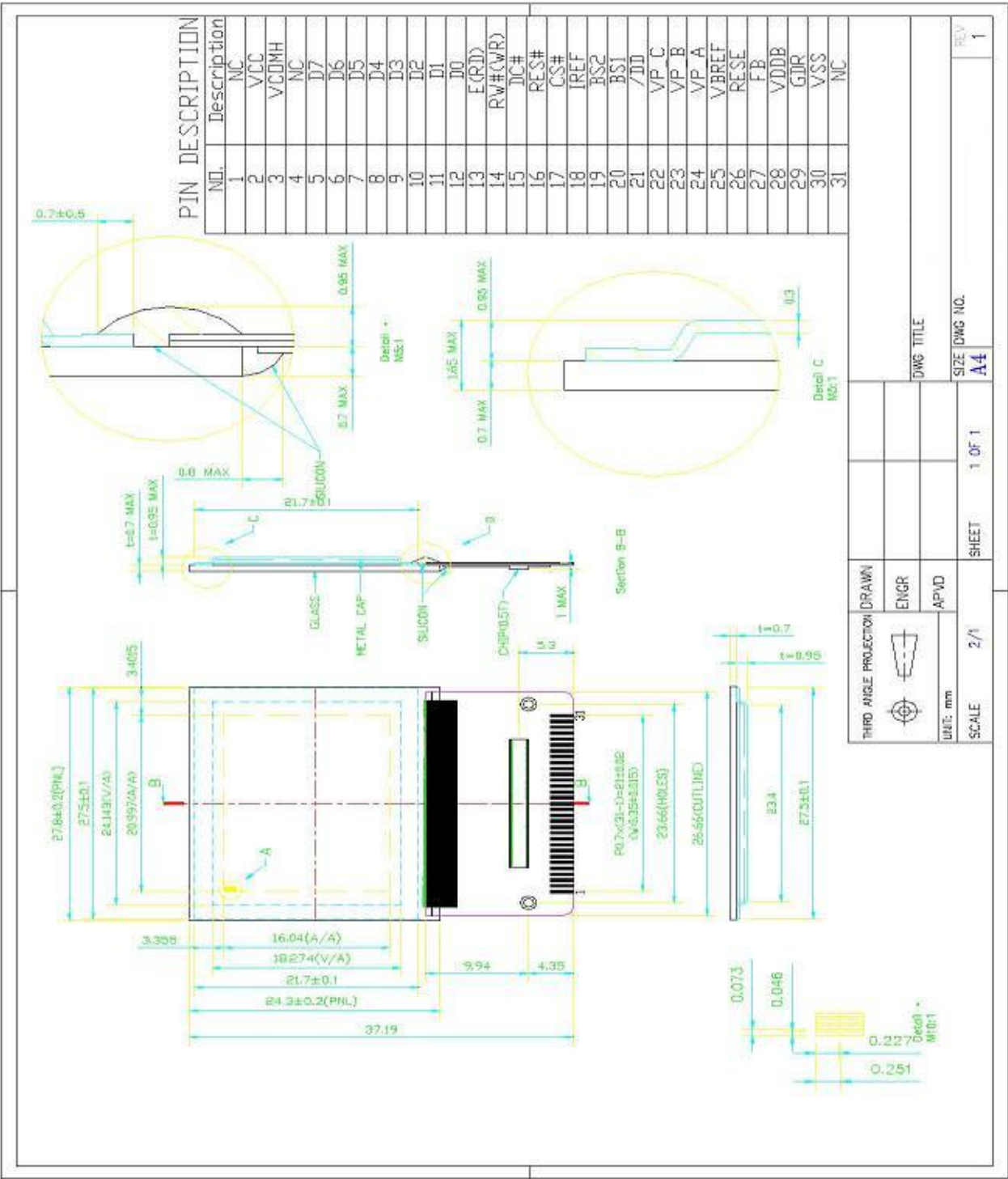
- ❶ The inspection standard and operation condition of customer are changed
- ❷ The new problems without being indicated in this specification
- ❸ The questions related to this specification
- ❹ The new problems occurred during the operation experiment.

12. 96xRGBx64 Color Panel

[Test Pattern]

(1) Full White	(5) Odd Line
	
(2) Full Red	(6) Even Line
	
(3) Full Green	(7) Frame
	
(4) Full Blue	
	

13. MECHANICAL DIAGRAM



14. PACKING DIAGRAM

NO	ITEM	CODE	SPEC	Q'ty	REMARK
1	MODULE		28*37.89*2.1	320 EA	
2	Sponge		395*265*5	2 EA	
3	Plastic-Tray		390*260*15	12 EA	
4	Sponge		260*110*5	2 EA	
5	Sponge		395*110*5	2 EA	
6	Box-Carton		399*269*123	1 EA	
7	Sponge		160*95*5	40 EA	

Scale: 3:1

32 EA / PP Tray
PP Tray: 10 EA

320 EA / Box

QA inspection label

The tape to seal carton

P.P. band

MADE IN TAIWAN

QA inspection label

90 40

QA inspection label

LOT NO.

BY: PQC

DATE