

PLED Module OSD2503M Product Specifications

1 Overview

OSD2503EM is a pLED monochrome dot matrix display module to be designed as consumer applications. The characteristics of this display module are self-emission, high brightness, high contrast ratio, slim/thin outline, and low panel power consumption.

2 Features

- Shift clock frequency: 5 MHz (Max.) ($V_{DD}=2.4\sim5.5V$)
- Series data input
- Supply voltage for OLED driver: 7 ~8V
- 4.0 cm (1.58 inch) diagonal
- 64 x 16 pixels
- Low power consumption
- 55 cd/m² typically
- High contrast ratio
- Compact, thin and light

3 Absolute maximum ratings

3.1 Electrical Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply voltage (Logic)	VDD	-0.5 to +7.0	V
Supply voltage (Driving buffer)	VLED	-0.5 to +10	V
DC Input voltage	V _I	-0.5 to V _{DD} +0.5	V
Power dissipation (Logic)	P _{D(max)}	3	mW
Power consumption(Panel)	P _(typical)	20 (Note 1)	mW

3.2 Environmental Absolute Maximum Ratings

Item	Operating		Storage		Comment
	Min.	Max.	Min.	Max.	
Ambient Temperature	-20°C	50°C	-30°C	70°C	
Humidity	45°C 85%RH		45°C 85%RH		(Note 2)
Corrosive gas	Not Acceptable		Not Acceptable		

Note 1. The value is the typical power consumption when quarter of pixels on.

Note 2. Damages of polarizer and adhesive tapes are not considered.

3.3 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Supply voltage (Logic)	3.0	3.3	5.5	V
VLED	Supply voltage (Driving buffer)	7		8	V
Top	Operating temperature	-20	25	50	°C

4 Electrical characteristics

4.1 DC characteristics

VDD=2.4 ~ 5.5V ; VSS=VSS2=0V ; VLED=8V ; Top=-20 ~ 50 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input high voltage	V _{IH}		2	-	-	V
Input low voltage	V _{IL}		-	-	0.8	V
Supply current	I _{CVDD}	Note3	-	-	1.0	mA
	I _{CVLED}				125	μA
Display OFF current	I _{CVDD}	Note4	-	-	1.0	mA
	I _{CVLED}				1.0	μA

4.2 AC characteristics

VDD=2.4 ~ 5.5V ; VSS=VSS2=0V ; VLED=8V ; Top=-20 ~ 50 °C

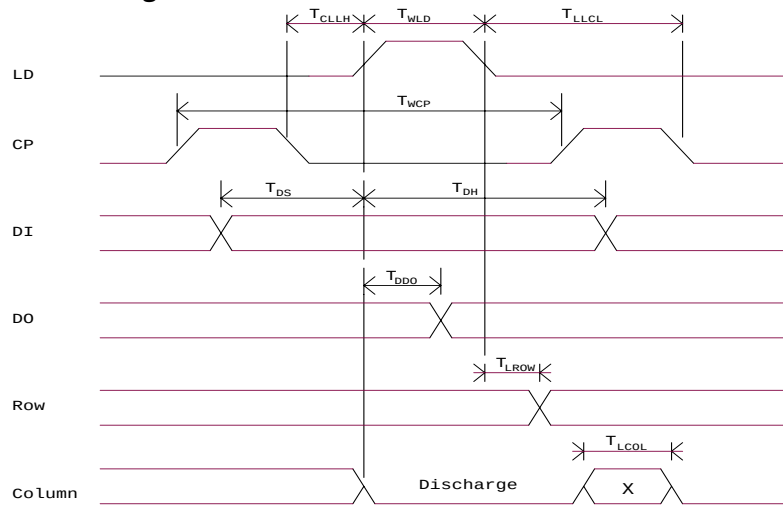
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Shift clock period	T _{WCP}		200	-	-	ns
Data latch in setup time	T _{DS}		40	-	-	ns
Data latch in hold time	T _{DH}		40	-	-	ns
CP low to LD high	T _{CLLH}		20	-	-	ns
LD low to CP low	T _{LLCL}		20	-	-	ns
LD 'H' pulse width	T _{WLD}		100	-	-	ns
LD low to Row output	T _{LROW}	Load=0.6nF	-	-	9	μs
LD high to column output	T _{LCOL}	Note5	-	-	-	ns
Output delay time	T _{DDO}	CL=15pF	40	-	100	ns

Note3 VDD = 3.0V, f_{CP} = 2.08 MHz, f_{LD}=12.8K Hz, No load. The input data is turned over by CP.

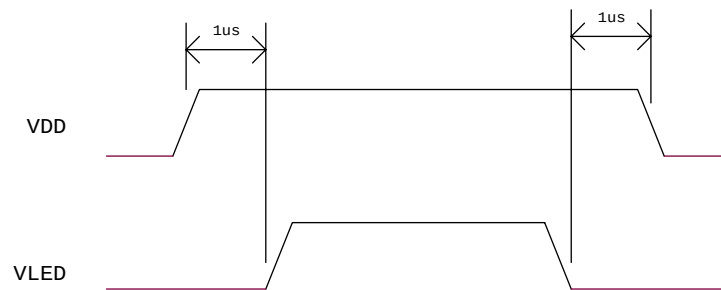
Note4 VDD = 3.0V, f_{CP} = 5 MHz, No load. The input data is turned over by CP. DISPOFF set to 'L'.

Note5 Depending on loading, please refer to DC characteristics

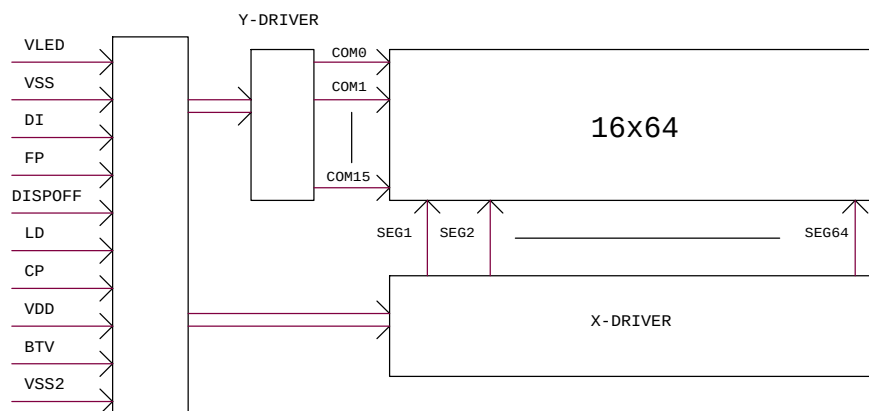
4.3 AC Timing



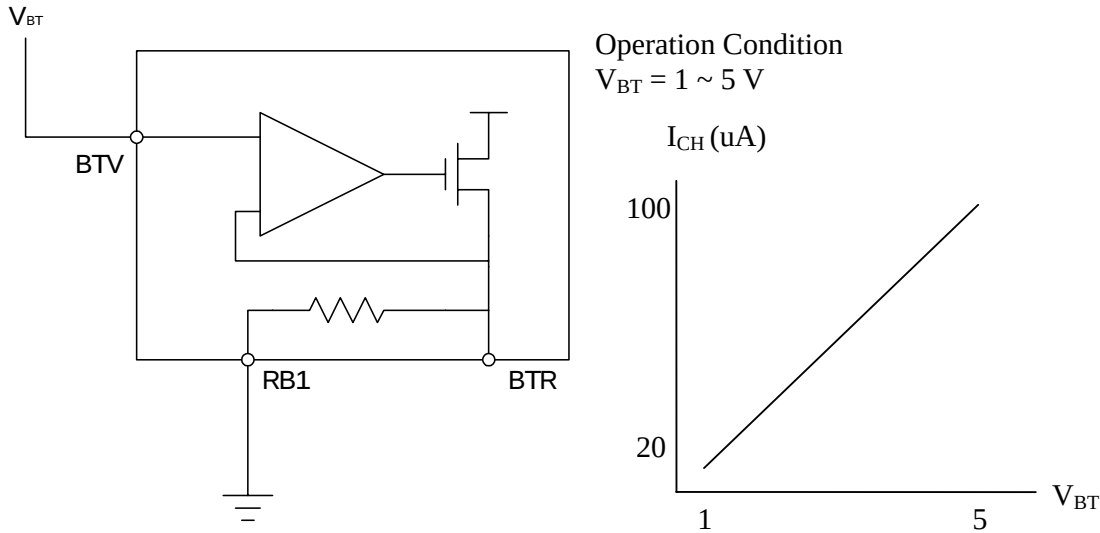
4.4 Power ON/OFF sequence



5 Block Diagram



5.1 Brightness Control



6 Interface Pin function

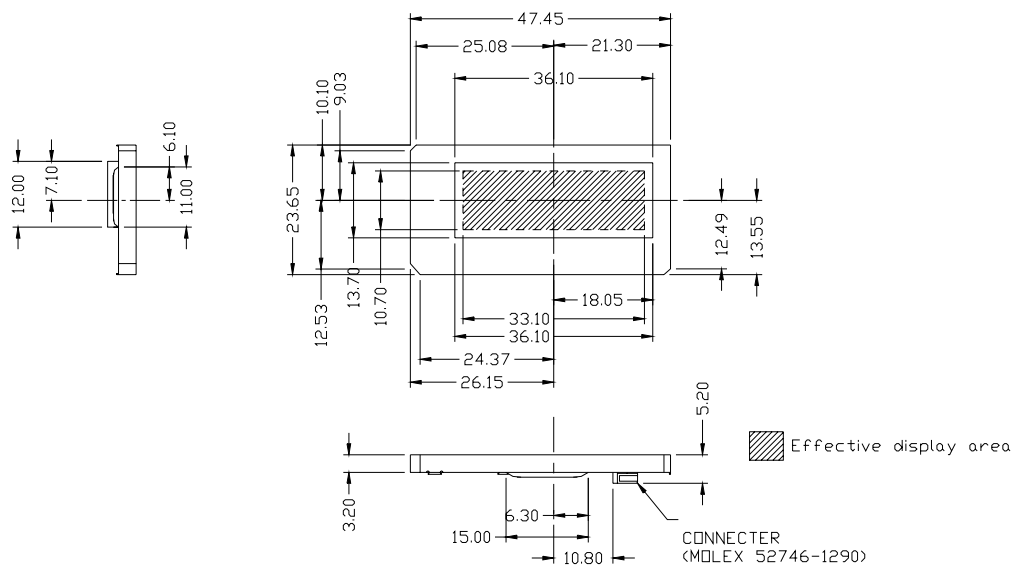
Mnemonic	Pin No.	I/O	Description
VLED	1,2	-	Power supply of pLED driving buffer
VSS	3	-	GND of digital circuit
DI	4	I	Series data inputs of column driver
FP	5	I	Frame start pulse, before a new frame
DISPOFF	6	I	Control for output deselect level While set to 'L', the driver outputs deselect level (VSS2). While set to 'H', the driver outputs constant current/voltage depending on mode selection.
LD	7	I	Data load pulse. When used as a column driver, a row of display data is latched at the falling edge of 'LD'.
CP	8	I	Data shift clock. The data is shifted to 64 bits shift register at the falling edge of 'CP' when used as column driver.
VDD	9	-	Power supply of digital circuit
BTV	10	I	Brightness control input. By adjusting an external voltage (V_{BT}), the output current in O[1:64] can be adjusted, see function description.
VSS2	11,12	-	GND of pLED driving buffer

7 Physical specifications

7.1 Mechanical specifications

NO.	Item	Specification	Unit
1	Display resolution	64x16	Pixels
2	Effective display area	33.10x13.5	mm
3	Panel size	46x22.60	mm
4	Dot size	0.4x0.35	mm
5	Dot pitch	0.65x0.50	mm
6	Module dimension	47.45*23.65	mm
7	Weight	4.9	g
8	Connector	Molex (52746-1290)	pcs

7.2 Drawing



8 Optical specifications

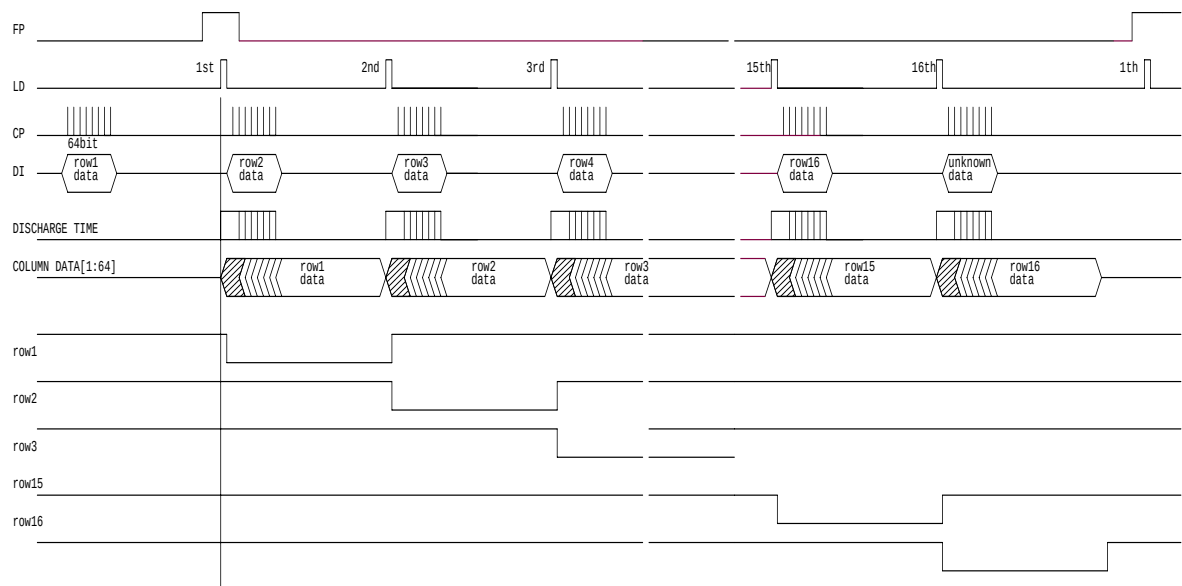
Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Response time	Rise			-	10	-	μs
	Fall			-	10	-	μs
Contrast ratio			100 lux	-	20	-	
Viewing angle	Top			-	80	-	deg
	Bottom			-	80	-	deg
	Left			-	80	-	deg
	right			-	80	-	deg

9 Reliability test items

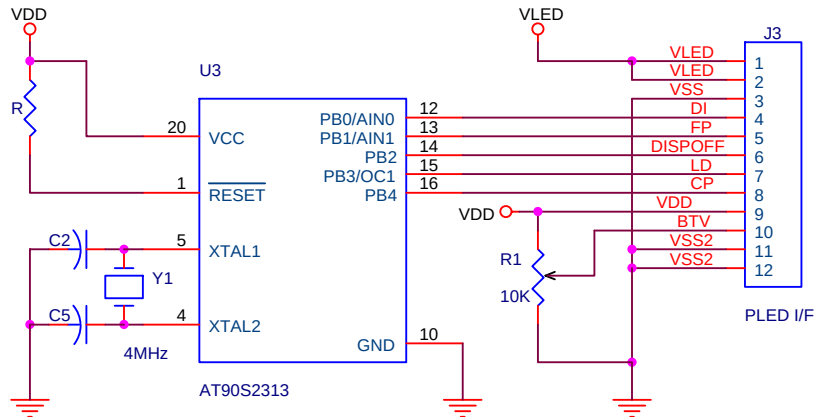
NO.	Test items	Conditions
1	High temperature storage	70°C , 240 hrs
2	Low temperature storage	-30°C,240 hrs
3	High temperature operation	50°C, 240 hrs
4	Low temperature operation	-20 °C, 240 hrs
5	High temperature and high humidity storage test	60°C, 90% RH, 240 hrs
6	High temperature and high humidity operating test	45°C, 85%RH, 240 hrs
7	Temperature Cycling (operating)	-20 °C (30 mins.) → 90 mins. → +50 °C (30 mins.) → 90 mins → -20 °C (30 mins.), 100 Cycles

10 Application Note

10.1 Programming Timing Chart



10.2 Circuit Example



10.3 Program

```

/*===== */
/* This Demo program will show a graphic on panel */
/*===== */
/* Project name : 16x64 CtrlBD for demo */
/* File name : demo1664.c */
/* MCU : AVR AT90s2313 */
/* Xtal : 4MHz */
/* Panel I/F : DI,FP,DISPOFF,LD,CP */
/* Writer : Leon Yu */
/* Date : 14/05, 2001 rev.A */

```

```

#include <io2313.h>
#include <pgmspace.h>

```

```

#define DI 0x01 // Data input pin
#define FP 0x02 // Frame pulse pin
#define DISPOFF 0x04 // Display On/Off pin
#define LD 0x08 // Latch pin
#define CP 0x10 // CP clock input pin
#define COLNO 64 // No. of column
#define ROWNO 16 // No. of row
#define MASK 0x80 // mask bit

```

```

void init(void);
void init(void)
{
    DDRB=0xff; // set PORTB as output
    PORTB=0x00; // set initial PORTB=0
}

```

```

// -----
// -- GRAPHIC --
// -----

```

```

flash unsigned char pattern[]={

```

```

    7, 240, 127, 246, 15, 225, 28, 0, //row 1
    7, 252, 127, 246, 15, 225, 28, 0, //row 2
    6, 14, 96, 6, 0, 96, 54, 0, //row 3
    6, 6, 96, 6, 0, 96, 54, 0, //row 4
    6, 3, 96, 6, 0, 96, 99, 0, //row 5
    6, 3, 96, 6, 0, 96, 99, 0, //row 6
    6, 3, 96, 6, 0, 96, 99, 0, //row 7
    6, 3, 127, 230, 0, 96, 193, 128, //row 8

```

```

6, 3, 127, 230, 0, 96, 193, 128, //row 9
6, 3, 96, 6, 0, 96, 255, 128, //row 10
6, 3, 96, 6, 0, 97, 255, 192, //row 11
6, 3, 96, 6, 0, 97, 128, 192, //row 12
6, 6, 96, 6, 0, 97, 128, 192, //row 13
6, 14, 96, 6, 0, 99, 0, 96, //row 14
7, 252, 127, 247, 252, 99, 0, 96, //row 15
7, 240, 127, 247, 252, 99, 0, 96, //row 16

```

```

};
void main(void)
{
    unsigned char bitcnt;
    unsigned char bdata;
    unsigned char col,row;
    unsigned char flash *ptr;

    init(); // initial IO port
    PORTB &=~(DISPOFF); //DISPLAY OFF
    PORTB |=DISPOFF; //turn on display
    for (;;)
    {
        PORTB |=FP; // FRAME start
        for (row=0;row<ROWNO;row++)
        {
            ptr=pattern; // read pattern address
            ptr=(ptr+(row<<3)); // read 1 byte data
            for (col=0;col<(COLNO/8);col++)
            {
                bdata=*(ptr+col);
                for (bitcnt=0;bitcnt<8;bitcnt++)
                {
                    PORTB =(bdata & (MASK>>bitcnt)) ? (PORTB | DI):(PORTB & (~DI));
                    PORTB |=CP; // set cp=high , create a CP pulse
                    PORTB &=~(CP); // set cp=low
                }
            } // end of column
            PORTB |= LD; // create a LD pulse
            PORTB &=~(LD);
            if(row==0)PORTB &=~(FP); // end of frame
        } // end of row
    }
}

```

10.4 80x51 Program

```

;===== */
;* This Demo program will show a graphic on the panel */
;===== */
;din =p1,7
;fp =p3.4
;dispoff=p3.5
;ld =p3.6
;cp =p3.7

row equ r1

org 0
sjmp main

main:
mov tmod,#00000001b ;use 16bit timer0 (mode1)
mov tl0,#8 ;65536-512+8(wait)=65032 (FE08)
mov th0,#0feh
mov ie,#0 ;diable interrupt
mov p3,#0

```

```

;dispo
setb p3.5
setb tcon.4 ;start timer0

refresh:
mov dptr,#table
mov row,#16

;fp rise
setb p3.4

next_row:
mov r6,#8

next_byte:
mov r7,#8
mov a,#0
movc a,@a+dptr
inc dptr

next_bit:
;din
mov p1,a
rl a

;pulse cp
setb p3.7
clr p3.7

djnz r7,next_bit
djnz r6,next_byte

call wait
;ld pulse
setb p3.6
clr p3.6

;fp fall
clr p3.4

;pulse cp
setb p3.7
clr p3.7
;pulse cp
setb p3.7
clr p3.7
;pulse cp
setb p3.7
clr p3.7
;pulse cp
setb p3.7
clr p3.7

djnz row,next_row
jmp refresh

wait:
;test tcon.5
jnb tcon.5,$

;reload timer0
mov tl0,#8
mov th0,#0feh
clr tcon.5

```

nop
ret

```
table:
DB      0,      0,      0,      0,      0,      0,      0,      0
DB      0,      0,      0,      0,      0,      0,      0,      0
DB      0,      0,     192,      0,      0,      0,      0,      0
DB     124,      0,     204,      0,      7,     192,     12,      0
DB     102,      0,     204,      0,     12,      96,     12,      0
DB      99,      60,     223,      60,     12,     111,     159,      60,
DB      99,     102,     204,      6,     12,     108,     204,     102,
DB      99,     126,     204,      62,     12,     108,     204,     102,
DB      99,      96,     204,     102,     12,     108,     204,     102,
DB     102,      98,     204,     102,     12,     108,     204,     102,
DB     124,      60,     199,      62,      7,     207,     135,      60,
DB      0,      0,      0,      0,      0,     12,      0,      0
DB      0,      0,      0,      0,      0,     12,      0,      0
DB      0,      0,      0,      0,      0,      0,      0,      0
DB      0,      0,      0,      0,      0,      0,      0,      0
DB      0,      0,      0,      0,      0,      0,      0,      0
end
```

11 Precaution in Design

- (1) Please do not give a stress on the module which cause damage on the metal, plastic, and pled glass.
- (2) Polarizer is easily scratched and should be carefully handled then. Please do not touch the polarizer use hard material, such as tweezers, pencil lead and glass. Please do not touch it by barehand.
- (3) This module is easily damaged when suffers from static discharge, please take care of static electricity and insure human body grounding.