



One Stop Displays Product Specification

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PLED Module OSD2401M Product Specifications

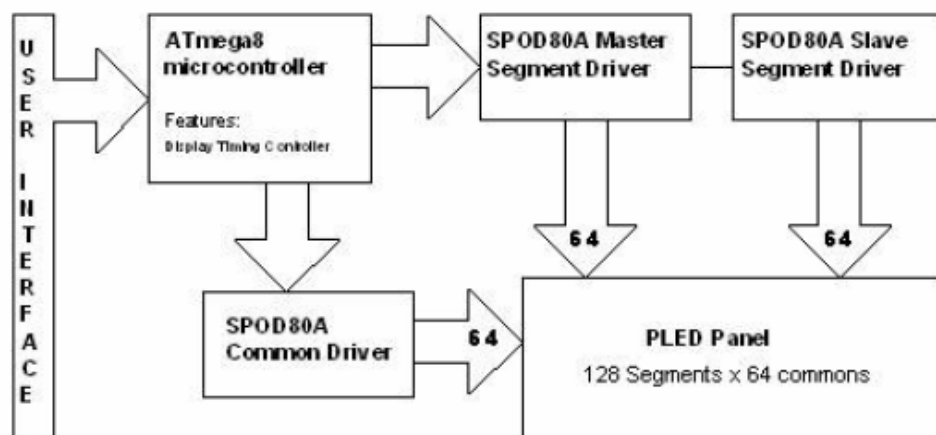
1. Overview

OSD2401M is a PLED monochrome dot matrix display module which is designed for consumer applications. Characteristics of this display module are self-emission, high brightness, high contrast ratio, lightweight, slim/thin outline, and low power consumption.

2. Features

- *Parallel data input*
- *Embedded timing controller*
- *128 x 64 pixels*
- *40 cd/m² typically*
- *High contrast image*
- *High uniformity*
- *High contrast ratio and wide viewing angle*
- *Compact, thin and light*

3. Block diagram



4. Absolute maximum ratings

4.1 Electrical Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage (Logic)	-0.5 to 5.5	V
V_{COL}	Supply voltage (Column driving buffer)	-0.5 to +18	V
V_{ROW}	Supply voltage (Row driving buffer)	-0.5 to +18	V
$P(\text{typical})$	Power consumption	0.4 ¹	W

4.2 Environmental Absolute Maximum Ratings

Item	Operation		Storage		Comment
	Min.	Max.	Min.	Max.	
Ambient	-20 °C	50 °C	-30 °C	70 °C	

¹ The value is the typical power consumption when quarter of pixels on.

4.3 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage (Logic)	2.8	3.3/5	5.5	V
V_{COL}	Supply for column voltage	10	13	15	V
V_{ROW}	Supply for row voltage	10	13	15	V
V_{REF}	Reference voltage	-	3	-	V
T_{OP}	Operating temperature		25		°C

Note: V_{ROW} is normally set that $V_{ROW} \geq V_{COL}$ to remove residual images.

Note: V_{COL} controls the brightness of the display.

5. Electrical characteristics

5.1 DC characteristics

$V_{DD}=2.8\sim 5.5V$; $V_{SS}=V_{SS2}=0V$; $V_{COL}=13V$; $V_{ROW}=13V$; $T_{OP}=-20 \sim 50^{\circ}C$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input low voltage	V_{IL}		-0.5	-	$0.2V_{DD}^2$	V
Input high voltage	V_{IH}		$0.6V_{DD}^3$	-	$V_{DD}+0.5$	V
Output low voltage	V_{OL}	$V_{DD}=5V$	-	-	0.7	V
		$V_{DD}=3.3V$			0.5	V
Output high voltage	V_{OH}	$V_{DD}=5V$	4	-	-	V
		$V_{DD}=3.3V$	2.2			V
Output high voltage	I_{vdd}	$V_{DD}=5V$	15 ⁴	-	17 ⁵	mA
	I_{col}		0.05 ⁴		12 ⁵	mA
	I_{row}		0.84 ⁴		15 ⁵	mA

5.2 AC timing

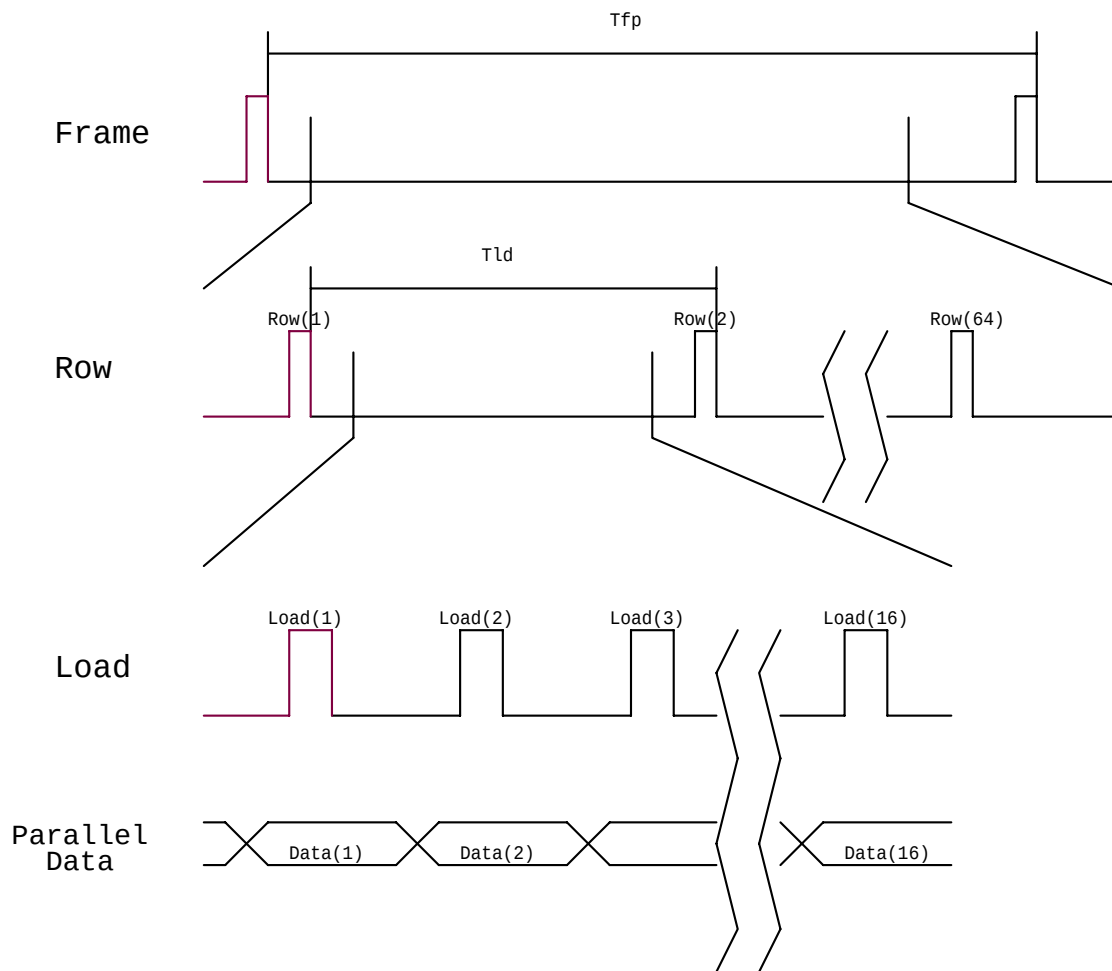
$V_{DD}=2.8\sim 5.5V$; $V_{SS}=V_{SS2}=0V$; $V_{COL}=13V$; $V_{ROW}=13V$; $T_{OP}=-20 \sim 50^{\circ}C$

² "Max" means the highest value where the pin is guaranteed to be read as low

³ "Min" means the lowest value where the pin is guaranteed to be read as high

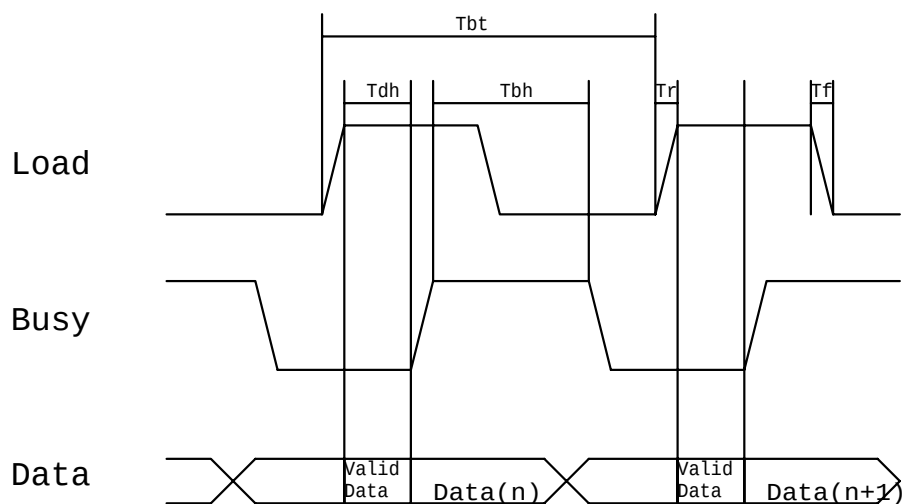
⁴ "Min" means the lowest value encountered when no pixels are activated; idle

⁵ "Max" means the highest value encountered when all pixels are activated



Parameter	Symbol	Min	Typ	Max	Unit
Frame start period	T_{fp}	-	13.33	-	ms
Row data loading period	T_{ld}	-	208.33	-	μs

5.3 Data loading timing

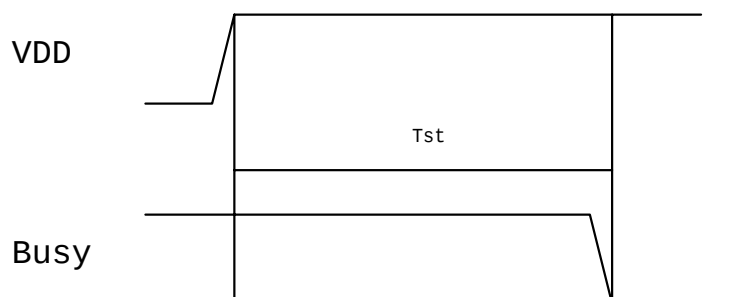


Parameter	Symbol	Min	Typ	Max	Unit
8 bits data transferring time	T_{bt}	-	13.02 ⁴	13.95 ⁵	μs
Valid data holding time	T_{dh}	1.25	1.50	-	μs
Busy holding time	T_{bh}	6.50	-	-	μs
Rising time	T_r	16	20	-	ns
Falling time	T_f	16	20	-	ns

⁴ For 75 frame rate

⁵ For 70 frame rate

5.4 Power on sequence



Parameter	Symbol	Min	Typ	Max	Unit
Time delay of pulling down busy flag when powering on	T_{st}	64	-	-	ms

Note: VDD must be applied with VCOL and VROW.

6. Interface pin function

Mnemonic	Pin No.	I/O	Description
V_{COL}	1	I	Power supply of PLED column buffer
V_{ROW}	2	I	Power supply of PLED row buffer
Gnd_Power	3	-	Analog ground
V_{DD}	4	I	Logic supply voltage
V_{REF}	5	I	Reference voltage
Gnd_Logic	6	-	Logic ground
Load	7	I	Data loading command Load='1': System loads 8 bits parallel data Load='0': System is busy; system operates
Reserved	8	I	Reserved pin
nReset	9	I	Negative reset function nReset='1': System operates (default) nReset='0': System reset; power up and delay for a while

Mnemonic	Pin No.	I/O	Description
Busy	10	O	Loading busy flag Busy= '1' : System is busy; System can't accept command Busy= '0': System idles; System can accept command
DB0~DB7	11~18	I	Parallel 8 bits data bus
NC	19~20	-	No connection

7. Display Data

● Graphic data

Graphic data construction is built bellow:7

b7 denotes (**Col1, Row1**) data while **b0** specifies (**Col8, Row1**).

Equally, **b7** denotes (**Col9, Row1**) data while **b0** specifies (**Col16, Row1**).

: : : : : : : : : : : : : : : : : :

Equally, **b7** denotes (**Col121, Row64**) data while **b0** specifies (**Col128, Row64**).

	Col1~Col8	Col9~Col16	Col17~Col24		Col113~Col120	Col121~Col128
Row1	(b7~b0)	(b7~b0)	(b7~b0)		(b7~b0)	(b7~b0)
Row2	(b7~b0)	(b7~b0)	(b7~b0)		(b7~b0)	(b7~b0)
Row3	(b7~b0)	(b7~b0)	(b7~b0)		(b7~b0)	(b7~b0)
	:					:
	:					:
	:					:
Row63	(b7~b0)	(b7~b0)	(b7~b0)		(b7~b0)	(b7~b0)
Row64	(b7~b0)	(b7~b0)	(b7~b0)		(b7~b0)	(b7~b0)

- Display addressing

The first 8 bits data is located in **(X1, R1)** and the next 8 bits data is followed in **(X2, R1)**.

The first row is completed when data is transferred to **(X16, R1)**. Then, **Row2** is followed by other 16 bytes data. A frame is completed when data of 16 rows is transferred.

	X1 Col1~Col8	X2 Col9~Col16	X3 Col17~Col24		X15 Col113~Col120	X16 Col121~Col128
Row1	(X1,R1)	(X2,R1)	(X3,R1)		(X15,R1)	(X16,R1)
Row2	(X1,R2)	(X2,R2)	(X3,R2)		(X15,R2)	(X16,R2)
Row3	(X1,R3)	(X2,R3)	(X3,R3)		(X15,R3)	(X16,R3)
	:					:
	:					:
	:					:
Row63	(X1,R63)	(X2,R63)	(X3,R63)		(X15,R63)	(X16,R63)
Row64	(X1,R64)	(X2,R64)	(X3,R64)		(X15,R64)	(X16,R64)

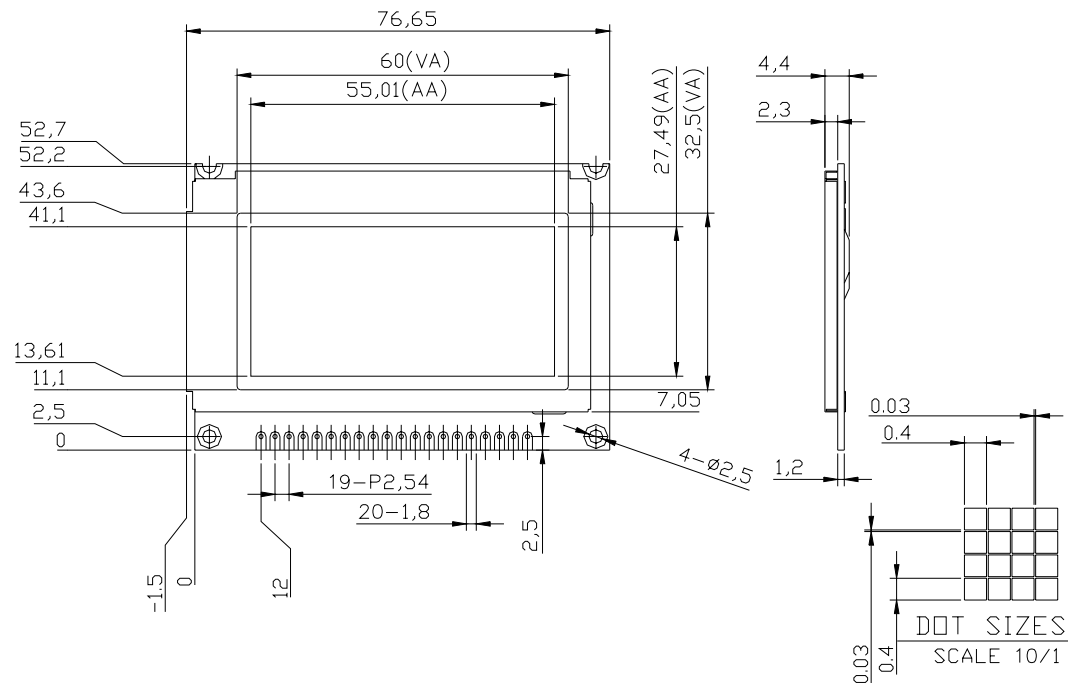
8. Physical specifications

8.1 Mechanical specifications

NO.	Item	Specification	Unit
1	Display resolution	128 x 64	Pixels
2	Module dimension	76.65 x 52.7 x 5.5 ⁶	mm
3	Viewing area(VA)	60.00 x 32.50	mm
4	Active area(AA)	55.01 x 27.49	mm
5	Dot size	0.4 x 0.4	mm
6	Dot pitch	0.43 x 0.43	mm
7	Weight	30	g

⁶ Length x Width x Height(including COB thickness)

8.2 Drawing



9. Optical specifications

$V_{DD}=2.8\sim5.5V$; $V_{SS}=V_{SS2}=0V$; $V_{COL}=13V$; $V_{ROW}=13V$; $T_{OP}=-20 \sim 50^{\circ}C$

Item		Condition	Min.	Typ.	Max.	Unit
Response time	Rise		-	10	-	us
	Fall		-	10	-	us
Contrast ratio			-	100:1	-	
Viewing angle	Top		-	80	-	deg
	Bottom		-	80	-	deg
	Left		-	80	-	deg
	right		-	80	-	deg
Color			-	YG ⁷	-	

⁷ YG=yellow green

10. Reliability

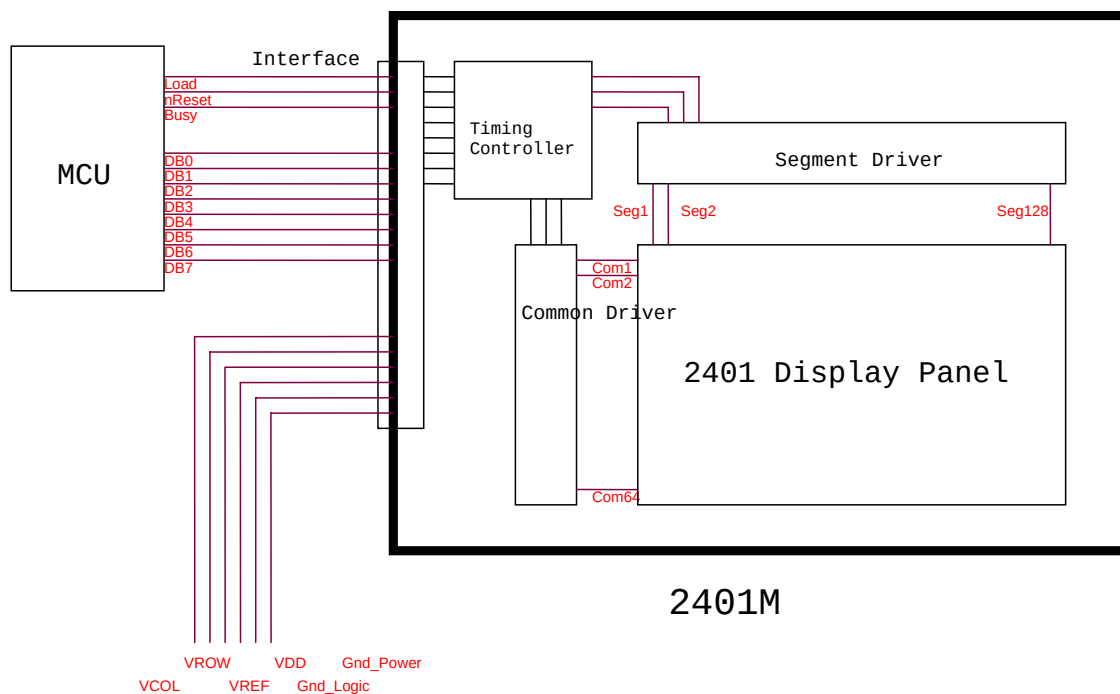
10.1 Reliability test item

NO.	Test items	Conditions
1	High temperature storage	70°C , 120 hrs
2	Low temperature storage	-30°C, 120 hrs
3	High temperature operation	50°C, 120 hrs
4	Low temperature operation	-20°C, 120 hrs
5	High temperature and high humidity storage test	40°C, 90% RH, 120 hrs
6	Thermal shock storage	-20°C (30 mins.) -->60°C/(30min), 20 Cycles

11. Application

11.1 Application circuit

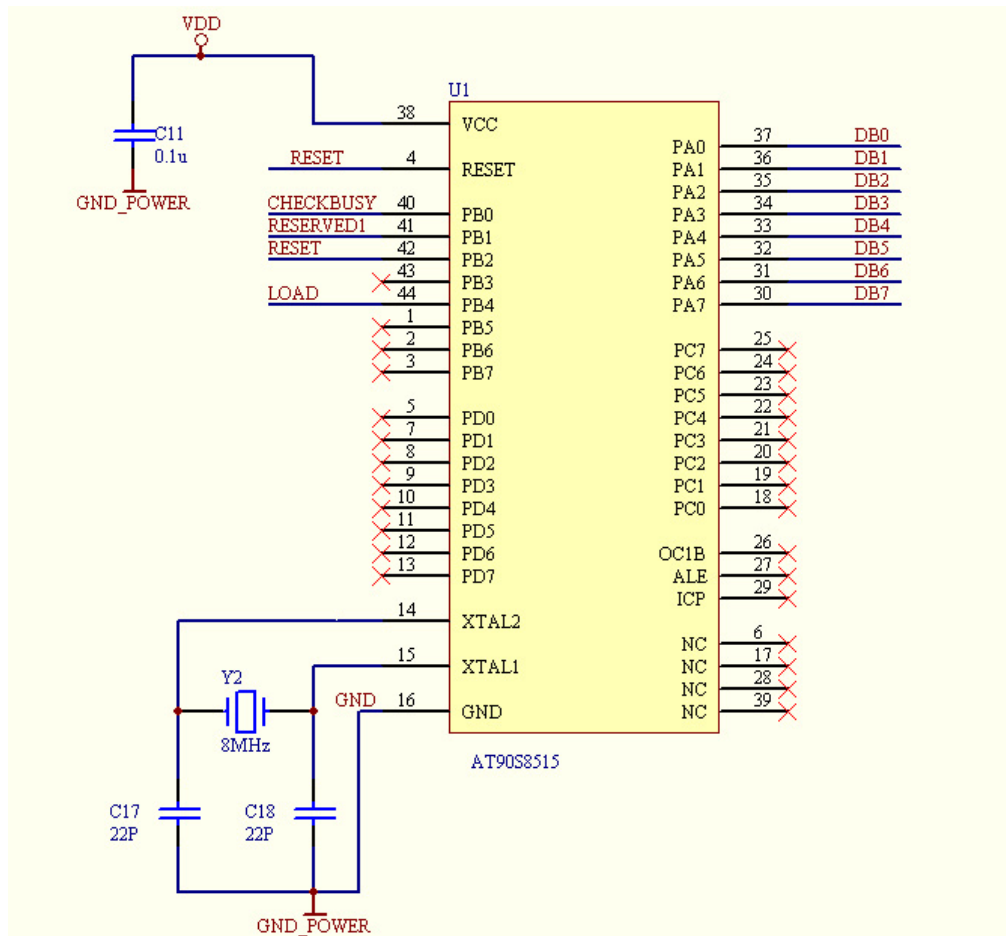
- Application example



● MCU Application

Controller: AVR AT90S8515

Oscillator: 8M Hz



11.2 Application program

```
.include "8515def.inc";include definition file
```

```
*****
```

```
;*Parameter Definition
```

```
*****
```

```
=====;Registor
```

```
definition
```

```
=====;def
```

```
tmpReg=R16
```

```
.def tmpReg2=R17
```

```
.def tmpReg3=R18
```

```
.def FrameRowNumberReg=R19
```

```
.def RowByteNumberReg=R20;
```

```
=====
```

```
;Control pin
```

```
=====
```

```
.equ Load=PB4;
```

```

.equ CheckBusy=PB5;
.equ Reset=PB3

;=====
;Constant definition
;=====

.equ FrameRowNumber=64
.equ RowByteNumber=16

;*****
;*Macro Definition
;*****
.macro StackPointer_Init
ldi tmpReg,low(ramend)
out SPL,tmpReg
ldi tmpReg,high(ramend)
out SPH,tmpReg
.endmacro

.org 0x00
rjmp Main

Main:
StackPointer_Init
rcall Port_Init
cbi PORTB,Reset;
cbi PORTB,Load

ldi tmpReg,2;Initial delay
rcall Delay;Initial delay

rjmp Display

;*****
;*Delay Function
;***** Delay:

;====Based on 8M oscillator, the execution time of StartDelay loop is 0.1 s
StartDelay:

ldi tmpReg,200
;====Based on 8M oscillator, the execution time of StartDelay2 loop is 500
us
StartDelay2:

ldi tmpReg,250
;====Based on 8M oscillator, the execution time of StartDelay3 loop is 2 us
StartDelay3:

nopl;1
nopl;2
nopl;3
nopl;4
nopl;5
nopl;6
nopl;7
nopl;8
nopl;9
nopl;10
nopl;11
nopl;12
nopl;13

dec tmpReg3; 14
brne StartDelay3; 16 (2 ck)

dec tmpReg2
brne StartDelay2

dec tmpReg
brne StartDelay

ret

;*****
;*Initial Function
;*****
Port_Init;;Port initialize
ldi tmpReg,0b11111111;PortA initialize
out DDRA,tmpReg
ldi tmpReg,0b11011111;;PortB initialize
out DDRB,tmpReg;
ldi tmpReg,0b00000000;;PortC initialize
out DDRC,tmpReg;
ldi tmpReg,0b00000000;;PortD initialize
out DDRD,tmpReg;
ret

;*****
;*Display
;*****
Display:

ldi ZL,low(Pattern*2);Load display pattern address
ldi ZH,high(Pattern*2);Load display pattern address
ldi FrameRowNumberReg,FrameRowNumber
NextRow:

ldi RowByteNumberReg,RowByteNumber

```



```
NextByte:                                .db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line22
lpm;Load display pattern data            .db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line23
adiw ZL,1                                .db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line24

out PortA,R0;Output display pattern data

                                           .db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line25
Idle;;Check Module Busy                  .db 0,121,228,250,7,0,128,244,0,64,0,0,0,0,0,0;line26
sbic PINB,CheckBusy;if CheckBusy=0, skip next instruction .db 0,69,4,37,8,185,204,132,198,231,51,153,152,11,140,0;line27
rjmp Idle                                .db 0,69,196,37,8,164,146,229,40,68,74,74,32,10,80,0;line28
sbi PORTB,Load                            .db 0,69,4,37,8,164,146,133,232,68,74,74,16,10,80,0;line29
                                           .db 0,69,4,47,136,164,146,133,8,68,74,74,8,10,80,0;line30
Idle1;;                                  .db 0,121,231,40,135,56,76,244,230,36,50,73,177,10,76,128;line31
sbis PINB,CheckBusy;if CheckBusy=1, skip next instruction .db 0,0,0,0,0,32,0,0,0,0,0,0,1,0,0,0;line32
rjmp Idle1
cbi PORTB,Load                            .db 0,0,0,0,0,32,0,0,0,0,0,0,1,0,0,0;line33
                                           .db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line34
dec RowByteNumberReg                     .db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line35
brne NextByte                             .db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line36
                                           .db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line37
dec FrameRowNumberReg                     .db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line38
brne NextRow                             .db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line39
                                           .db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line40

rjmp Display;Continue to display

                                           .db 0,0,0,0,0,64,128,0,0,0,0,0,0,0,0,0,0;line41
                                           .db 0,0,0,0,0,64,144,0,0,0,0,0,0,0,0,0,0;line42
                                           .db 0,9,41,41,33,204,187,129,156,230,6,103,224,233,32,0;line43
                                           .db 0,5,69,69,66,82,144,66,82,73,8,148,144,69,64,0;line44
                                           .db 0,5,69,69,66,94,145,218,82,73,8,148,144,69,64,0;line45
                                           .db 0,2,130,130,130,80,146,66,82,73,8,148,144,66,128,0;line46
                                           .db 0,2,130,130,137,206,139,193,156,38,38,100,146,34,128,0;line47
                                           .db 0,0,0,0,0,0,0,16,0,0,0,0,0,0,0,0;line48

;*****
;*Pattern
;*****
Pattern:
.db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line1
.db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line2
.db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line3
.db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line4
.db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line5
.db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line6
.db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line7
.db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line8

                                           .db 0,0,0,0,0,0,0,16,0,0,0,0,0,0,0,0;line49
                                           .db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line50
                                           .db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line51
                                           .db 0,0,0,0,128,0,0,0,0,0,0,0,0,0,0,0;line52
                                           .db 0,0,1,240,128,99,8,56,28,78,6,127,223,0,0,0;line53
                                           .db 0,0,0,76,144,148,144,4,16,129,9,10,66,0,0,0;line54
                                           .db 0,0,0,82,128,99,56,8,25,194,9,8,130,0,0,0;line55
                                           .db 0,0,0,94,128,148,165,133,133,33,105,16,132,0,0,0;line56

.db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line9
.db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line10
.db 15,252,31,253,224,255,243,224,0,63,195,255,63,252,127,128;line11
.db 15,255,31,253,224,255,247,240,0,255,243,255,191,253,255,224;line12
.db 15,15,30,1,224,15,7,240,0,240,243,195,195,193,225,224;line13
.db 15,7,158,1,224,15,7,240,1,224,123,195,195,195,192,240;line14
.db 15,7,159,249,224,15,15,120,1,224,123,195,195,195,192,240;line15
.db 15,7,159,249,224,15,15,120,1,224,123,255,131,195,192,240;line16

                                           .db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line61
                                           .db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line62
                                           .db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line63
                                           .db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line64

.db 15,7,158,1,224,15,30,124,1,224,123,255,3,195,192,240;line17
.db 15,15,30,1,224,15,31,252,0,240,243,192,3,193,225,224;line18
.db 15,255,31,253,255,143,31,252,0,255,243,192,3,193,255,224;line19
.db 15,252,31,253,255,143,60,30,0,63,195,192,3,192,127,128;line20
.db 0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0;line21
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